

INTEL(R) E7500 High Performance Appliance Platform
-Intel(R) XEON(TM) Processor or Low Voltage Intel (R)
XEON(TM) Processor with 512 KB L2 Cache

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CPU BOARD SCHEMATIC
rev 1.01

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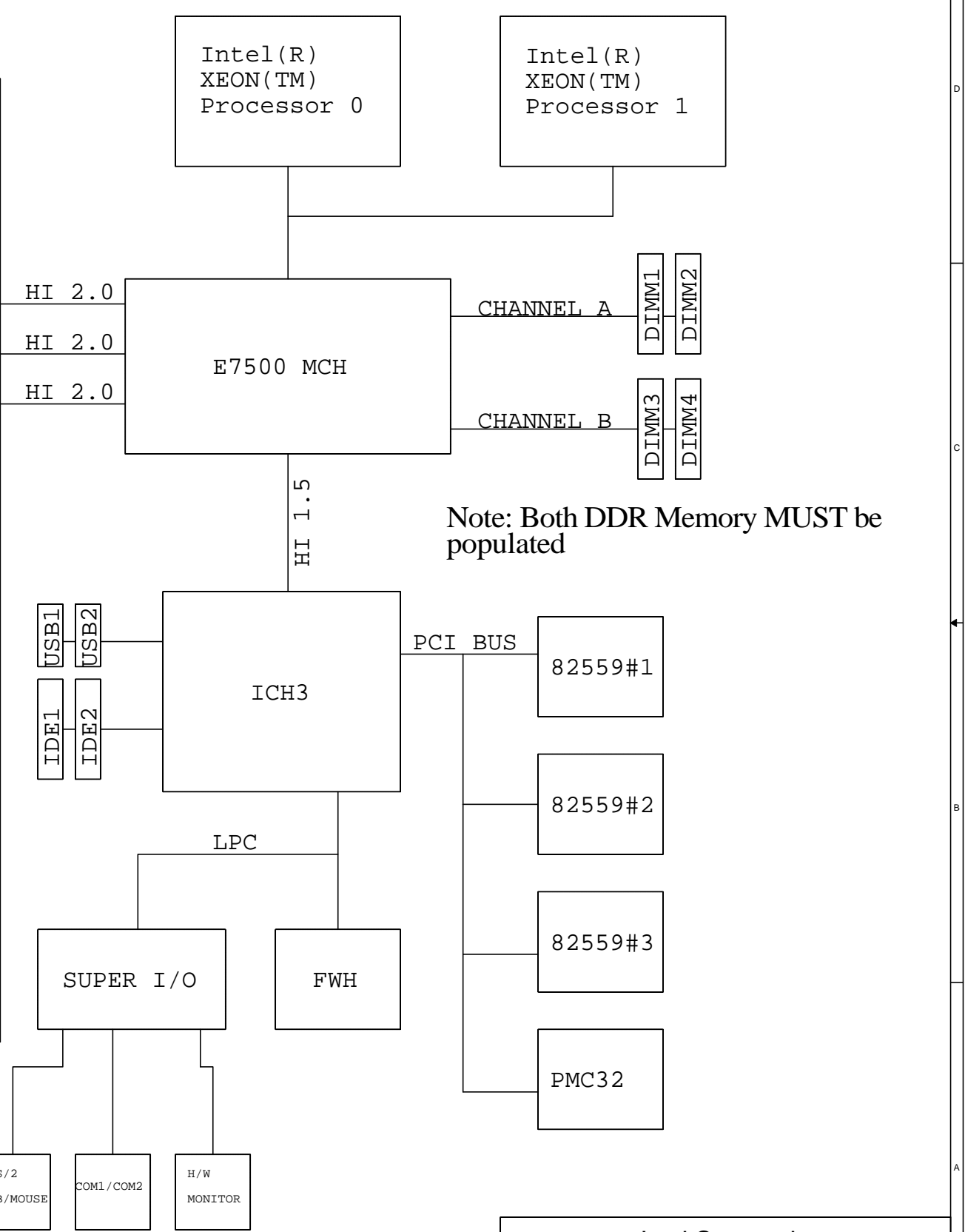
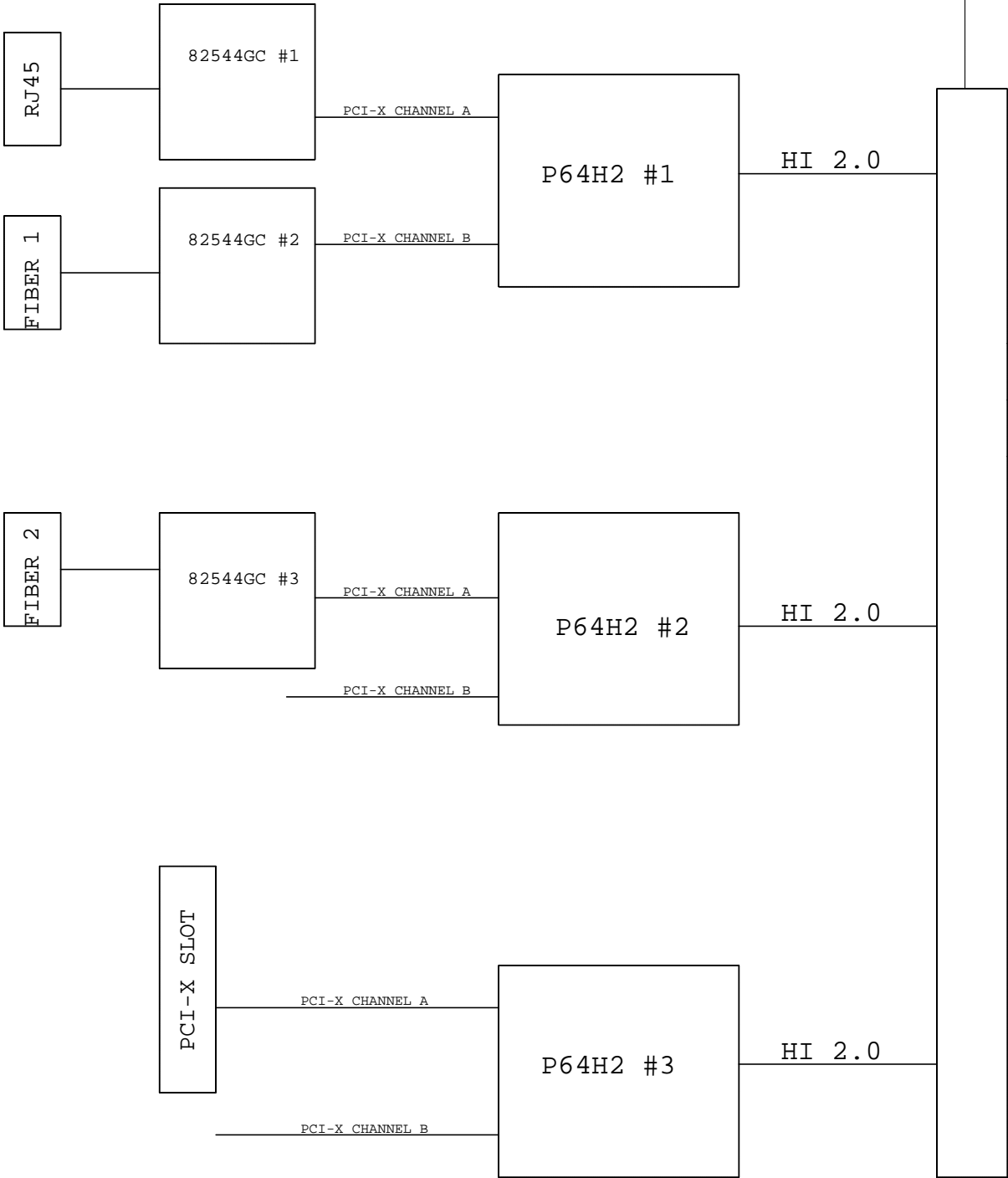
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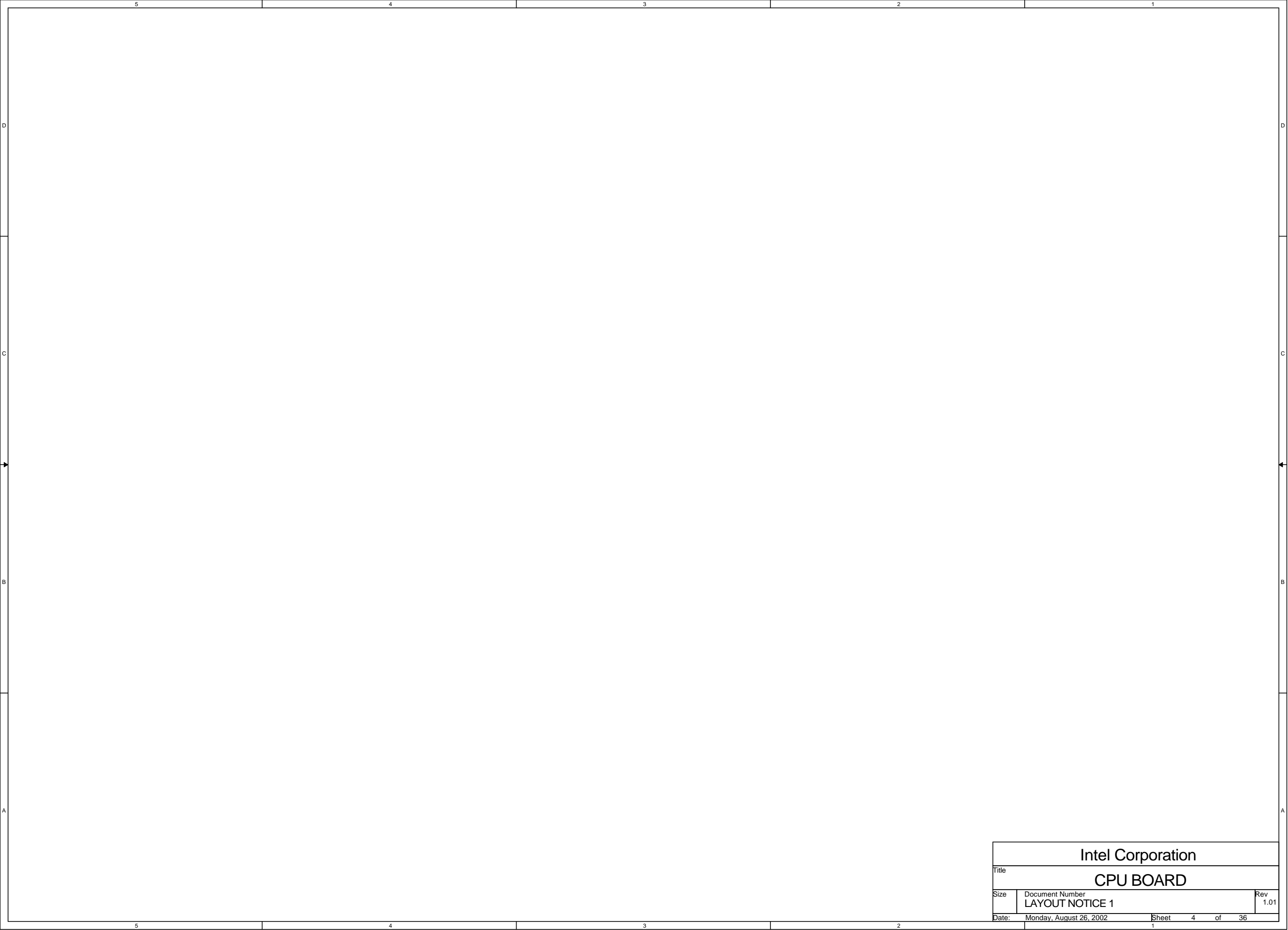
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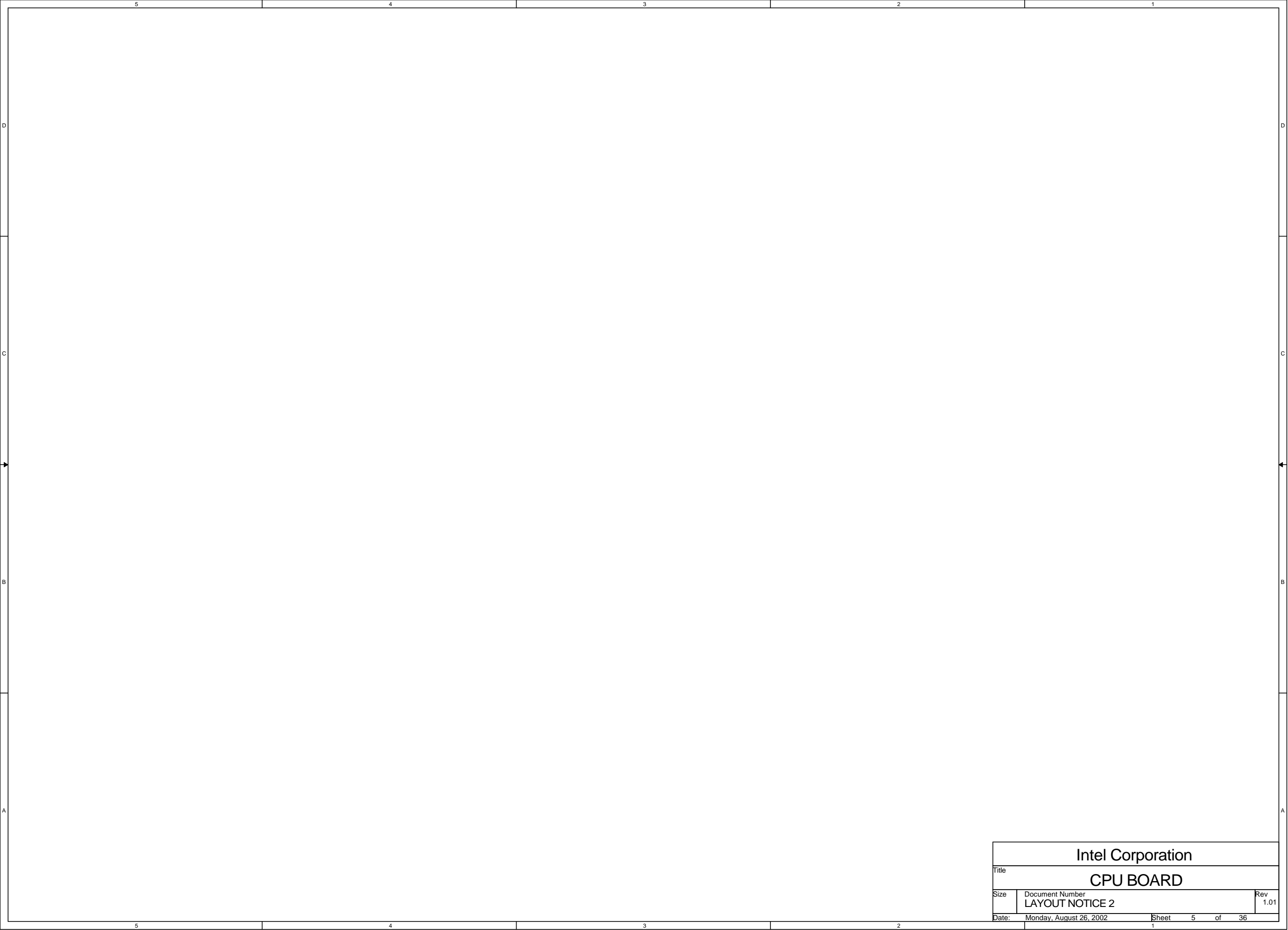
I/O BOARD

CPU BOARD



Note: Both DDR Memory MUST be populated





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CONNECTORS:

J1: ITP PORT
J2: COPPER GIGABIT PORT
J3: FIBER GIGABIT PORT
J4: FIBER GIGABIT PORT
J5: PCI-X SLOT
J6: USB PORT
J7: USB PORT
J8: RESET BUTTON
J9: COM1 PORT
J10: POWER BUTTON
J11: PS/2 KB/MOUSE
J12: 10/100M BITS RJ45
J13: 10/100M BITS RJ45
J14: 10/100M BITS RJ45
J15: LEDS CONNECTOR
IDE1: PRIMARY IDE CONNECTOR
IDE2: SECONDARY IDE CONNECTOR
ATX1: ATX POWER CONNECTOR
CPUFAN1: CPU FAN POWER CONNECTOR
CPUFAN2: CPU FAN POWER CONNECTOR

INTERRUPT ROUTING
TABLES:

ICH3 INTERRUPT:	P64H2#1
PIRQA#:	P64H2#1
PIRQB#:	P64H2#2
PIRQC#:	P64H2#3
PIRQD#:	NO USE
PIRQE#:	82559#1
PIRQF#:	82559#2
PIRQG#:	82559#3
PIRQH#:	NO USE

GPIO FOR LED CONTROL

GPIO34: LED CONTROL FOR POWER LED
GPIO35: LED CONTROL FOR CPU OVER HEAT LED
GPIO36: LED CONTROL FOR PRIMARY HDD LED
GPIO37: LED CONTROL FOR SECONDARY HDD LED
GPIO38: LED CONTROL FOR 10/100M BIT PORT1 ACTIVITY LED
GPIO39: LED CONTROL FOR 10/100M BIT PORT2 ACTIVITY LED
GPIO40: LED CONTROL FOR 10/100M BIT PORT3 ACTIVITY LED
GPIO41: LED CONTROL FOR GIGABIT PORT1 ACTIVITY LED
GPIO42: LED CONTROL FOR GIGABIT PORT2 ACTIVITY LED
GPIO43: LED CONTROL FOR GIGABIT PORT3 ACTIVITY LED

JUMPERS:

JP1: DP/UP SELECTION FOR ITP PORT
1-2 DP DEFAULT
2-3 UP
JP2: CPU SAFE MODE
ON ENABLE DEFAULT
OFF DISABLE
JP3: CLEAR CMOS
1-2 NORMAL DEFAULT
2-3 CLEAR CMOS
JP4: ICH3 TCO TIMER
ON DISABLE
OFF ENABLE DEFAULT
JP5: VRM ID SELECTION
JP6: CPU FAN POWER
1-2 +12V
2-3 5V

P64H2#3:	
P3AIRQ0:	PCI-X SLOT
P3AIRQ1:	PCI-X SLOT
P3AIRQ2:	PCI-X SLOT
P3AIRQ3:	PCI-X SLOT

